Design rules-1

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Why we need design rules

Design rules for a process are formulated to minimize the occurrence of common fabrication problems and bring the yield of correct chips to an acceptable level

- Better area efficiency
- Better yield
- Better reliability
- Increase the probability of fabricating a successful product on Si wafer

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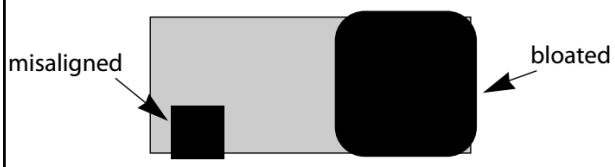
What's happened?



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Design rules and yield

- Design rules are determined by manufacturing process characteristics.
- Design rules should provide adequate yield if followed.
- Types of design rules:
  - Industry Standard: Micron Rule
  - λ Based Design Rules
- *Spacing, Separation, Composition*.

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Design rules and yield…

- Minimum length or width of a feature on a layer is 2 λ
  - To allow for shape contraction
- Minimum separation of features on a layer is 2 λ
  - To ensure adequate continuity of the intervening materials.

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Manufacturing problems

- Photoresist shrinkage, tearing.
- Variations in material deposition.
- Variations in temperature.
- Variations in oxide thickness.
- Impurities.
- Variations between lots.
- Variations across a wafer.

→
- Transistor problems
- Wiring problems
- Oxide problems
- Via problems

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Transistor problems

- Varaiations in threshold voltage:
  - oxide thickness;
  - ion implanatation;
  - poly variations.
- Changes in source/drain diffusion overlap.
- Variations in substrate.

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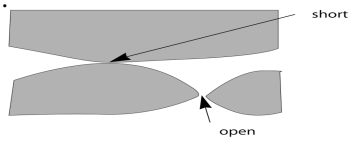
Wiring problems

- Diffusion: changes in doping -> variations in resistance, capacitance.
- Poly, metal: variations in height, width -> variations in resistance, capacitance.
- Shorts and opens:



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Oxide problems

- Variations in height.
- Lack of planarity -> step coverage.

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Via problems

- Via may not be cut all the way through.
- Undesize via has too much resistance.
- Via may be too large and create short.

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Design rules

- Industry Standard: Micron Rule
  - All device dimensions are expressed in terms of absolute dimension(μm/nm)
  - These rules will not support proportional scaling
- λ Based Design Rules (Developed by Mead & Conway)
  - All device dimensions are expresses in terms of a scalable parameter λ.
  - λ = L/2; L = The minimum feature size of transistor
  - these rules support proportional scaling.

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Scaling theory

- In digital circuit design scaling is possible because the capacitive loads that must be driven by logic gates shrink faster than the currents supplied by the transistors.
- Classical scaling theory runs into complications at nanometer features.
  - Leakage.
  - Smaller supply voltage.

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Scaling model

Assume that all the basic physical parameters of the chip are shrunk by a factor *1/x*:

- $\lambda \rightarrow \lambda$ /x.
- W $\rightarrow$ W/x, L $\rightarrow$ L/x.
- $t_{ox} \rightarrow t_{ox}$ /x.
- $N_d \rightarrow N_d$/x.
- $V_{DD} - V_{SS} \rightarrow (V_{DD} - V_{SS})$/x.

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Current and capacitance scaling

$\hat{k}'/k' = x \quad \hat{V}_t = V_t/x$

$$\frac{\hat{I}_d}{I_d} = \left(\frac{\hat{k}'}{k'}\right)\left(\frac{\hat{W}/\hat{L}}{W/L}\right)\left[\frac{(\hat{V}_{gs}-\hat{V}_t)^2}{(V_{gs}-V_t)^2}\right]$$

$$= x\left(\frac{1/x}{1/x}\right)\left(\frac{1}{x}\right)^2 = \frac{1}{x}$$

- Saturation drain current scales as 1/x.
- Capacitance scales as 1/x.
- Total performance over scaling:
  - [C'V'/l']/[CV/l] = 1/x

So, as the layout is scaled from λ to $\hat{\lambda} = \lambda/x$, ***the circuit is actually speeded up by a factor "x"***

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Interconnect scaling

- Two varieties of interconnect scaling:
  - **Ideal scaling** reduces vertical and horizontal dimensions equally: *the resistance increases with scaling*.
  - **Constant dimension** does not change wiring sizes: *resistance remains same*.
  - Higher levels of interconnect are constant dimension---same as older technologies.

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Quize

Predict how metal 1 and metal 2 resistance would change for a 90 nm process using:

- a) Ideal scaling.
- b) Constant dimension scaling

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